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REMARKS

Claims 2, 4-17 and 19-31 are pending the above-referenced patent application. In this response, claims 2 and 17 have been amended, and no claims have been added or cancelled. It is noted that claims 2 and 17 were amended to clarify intended subject matter. Accordingly, it is respectfully requested that the Examiner enter the amendments to claims 2 and 17.

Claim Rejections – 35 U.S.C §103(a)

The Examiner has rejected claims 2, 4-17 and 19-31 under 35 U.S.C. 103(a) as being unpatentable over Grisamore (U.S. Patent No. 6,535,901, hereinafter "Grisamore"); and has rejected claims 2, 4-17 and 19-31 under 35 U.S.C. 103(a) as being unpatentable over Costa (U.S. Patent No. 5,935,201, hereinafter "Costa"). These rejections are respectfully traversed. Reconsideration of the above-referenced patent application in view of the following remarks and foregoing amendments is respectfully requested.

Claim Rejections - 35 U.S.C. 103(a)

Grisamore

It is noted that in order to establish *prima facie* obviousness there must be some suggestion or motivation to modify or combine reference teachings, and the modification or combination, if successful, must teach or suggest all of the claim limitations. As stated in the Manual for Patent Examining Procedure (MPEP), § 2142/2143, "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." It

is respectfully submitted that the cited reference does not meet these criteria. For example, Grisamore, even if successfully modified, would still not teach or suggest all the claim limitations.

As just an example, Grisamore does not teach or suggest at least "a Wallace-architecture of full-adders to receive at least a portion of the one or more groups of three bits, half-adders to receive at least a portion of the one or more the groups of two bits, associated registers to receive at least a portion of the one or more the groups of one bit in the selected resources, and a multi-input adder to combine the input terms to produce intermediate summation results", as recited in claim 2. For example, Grisamore clearly describes passing partial products from the reduction tree module 18 to an adder 14 which is external from the reduction tree module. See, for example, col 3:28 – col 3:30 and Figure 1 of Grisamore. Accordingly, Grisamore does not teach or suggest a Wallace-architecture including "a multi-input adder to combine the input terms to produce intermediate summation results" because adder 14 of Grisamore is clearly not part of a Wallace-architecture, as set forth in claim 2, Grisamore has at least one deficiency, and fails to teach or suggest all the claim limitations of claim 2. Therefore, because a sufficient showing of obviousness has not been established, claim 2 is in a condition for allowance. Additionally, claims 4-17 and 19-31 either depend from or include limitations similar to those present in claim 2, and are, therefore, in a condition for allowance on at least the same basis.

Further, it is noted that the Examiner concedes that Grisamore is lacking at least one element of the rejected claims. According to the Examiner, "It is noted that Grisamore does not teach registers in figure 5. However, Grisamore discloses in col 1, lines 33-40 that it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply accumulate circuit." However, Grisamore clearly describes passing partial products from the reduction tree to an adder to perform adding functions, and passing and subsequently retrieving carry terms from a memory device [Col. 2:63-3:8.], rather than utilizing an apparatus having associated registers. Assignee is unable to find any description throughout Grisamore of registers implemented in a manner as recited in the rejected claims. The cited portion of Grisamore, referenced from the Background section, describe registers implemented in an array multiplier [Col. 1:33 – 1:41]. It is

respectfully requested that the Examiner either cite the portion of Grisamore that describes registers implemented as part of a Wallace-architecture, as recited in claim 2, or withdraw the rejection.

It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that this ground is sufficient. Assignee respectfully submits that because Grisamore has at least one deficiency, and fails to teach or suggest all the claim limitations of the rejected claims, a sufficient showing of obviousness has not been established. Accordingly, all pending claims are in a condition for allowance. It is respectfully requested that the Examiner withdraw his rejections of these claims.

Costa

It is respectfully submitted that Costa fails to meet the criteria set forth above to establish *prima facie* obviousness. For example, Costa, even if successfully modified, would still not teach or suggest all the claim limitations.

As just an example, Costa does not teach or suggest at least "a Wallace-architecture of full-adders to receive at least a portion of the one or more groups of three bits, half-adders to receive at least a portion of the one or more the groups of two bits, associated registers to receive at least a portion of the one or more the groups of one bit in the selected resources, and a multi-input adder to combine the input terms to produce intermediate summation results", as recited in claim 2. For example, Costa describes a multiplier circuit to produce a final sum of partial products by use of a final adder. In Costa, a multiplier circuit is described wherein input terms are combined, and partial products are generated [col 7: 39– 8:8 and Fig. 1]. The partial products are passed to a combinatorial network [col 9:29- 9:54 and Fig. 7] which performs the final adding of the partial products. It is respectfully submitted that there is no teaching or suggestion in Costa of at least "a Wallace-architecture of full-adders to receive at least a portion of the one or more groups of three bits, half-adders to receive at least a portion of the one or more the groups of two bits, associated registers to receive at least a portion of the one or more the groups of one bit in the selected resources, and a multi-input adder to combine the input terms to produce intermediate summation results", as recited in claim 2. Because

Costa has at least one deficiency, and fails to teach or suggest at least one limitation of claim 2, a sufficient showing of obviousness has not been established. Accordingly, claim 2 is in a condition for allowance. Additionally, claims 4-17 and 19-31 either depend from or include limitations similar to those present in claim 2, and are, therefore, in a condition for allowance on at least the same basis.

The Examiner concedes that Costa is lacking at least one element of the rejected claims. According to the Examiner, "It is noted that Costa et al does not teach registers in the Wallace-architecture. However, since it is known in the art to use registers at optimal points in a multiplier to enable pipelined processing which provides a high through put multiply circuit, it would have been obvious to a person of ordinary skill in the art to provides the Wallace-architecture of Costa et al. with registers at optimal points in the architecture to enable pipelined processing in order to increase the through put of circuit." However, as noted previously, the cited portions of Costa describe a multiplier circuit wherein input terms are combined, and partial products are generated [Col 7:39–8:8 and Fig. 1]. The partial products are passed to a combinatorial network [col 9:29-col 9:54 and Fig. 7] which performs the final adding of the partial products. Assignee is unable to find any description throughout Costa wherein registers implemented in a manner as recited in the rejected claims. Accordingly, it is respectfully requested that the Examiner either cite the portion of Costa that describes registers implemented as part of a Wallace-architecture, as recited in claim 2, or withdraw the rejection.

It is noted that many other bases for traversing the rejection could be provided, but Assignee believes that this ground is sufficient. Assignee respectfully submits that because Costa has at least one deficiency, and fails to teach or suggest all the claim limitations of the rejected claims, a sufficient showing of obviousness has not been established. Accordingly, all pending claims are in a condition for allowance. It is respectfully requested that the Examiner withdraw his rejections of these claims.

CONCLUSION

In view of the foregoing, it is respectfully submitted that all of the claims pending in this patent application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 439-6500. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Please charge any shortages and credit any overcharges of any fees required for this submission to Deposit Account number 50-3703.

Respectfully submitted,

Dated: 1/3/07

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I hereby certify that this correspondence is being submitted via facsimile or deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

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Date of Transmission

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